REMARKS

The Examiner's Action mailed on July 14, 2006 has been received and its contents carefully considered.

Claims 1-17 are pending in this application. In this Amendment, Applicant is amending claims 1, 4 and 12, and adding new claim 18. For at least the following reasons, it is submitted that this application, as amended, is in condition for allowance.

In the Action, claims 1-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Eide et al. (U.S. Patent No. 6,529,978). The rejection is respectfully traversed.

Regarding independent claim 1, the Examiner points to Eide as disclosing a computer system comprising: a system processor (Fig. 2, element 12); an input/output processor (Fig. 2, element 44); and an input/output adaptor (Fig. 2, element 46), connected to the system processor and the input/output processor, and capable of dynamically switching between being controlled by the system processor and being controlled by the input/output processor (Fig. 12).

The Applicant respectfully disagrees. Anticipation, under 35 U.S.C. §102, requires each element of the claim in issue be found in a single prior art reference, and that all limitations of the claim must be found in the reference. The Eide patent is directed to embodiments that support the dynamic reassignment of an input/output adapter (IOA) in a hierarchical I/O interface from

one input/output processor (IOP) to another IOP such that the latter IOP takes over management of data transfer from the former IOP (see column 2, lines 47-52, emphasis added). As shown in Figure 1 of Eide, each location 20 on bus 18 is configured to receive an input/output processor (IOP) or an input/output adapter (IOA) (see column 4, lines 40-42). The invention in Eide supports bindings between IOA's and IOP's that that can be changed without having to power off any part of the computer, and without having to physically move any IOA or IOP (see column 6, lines 28-32). Figure 12, relied upon by the Examiner, discloses the process for transferring the control of an IOA from one IOP to another IOP when the former IOP fails. However, contrary to the Examiner's position, Eide fails to teach a significant limitation of the present invention recited in claim 1, namely, "an input/output adaptor ... capable of dynamically switching between being controlled by the system processor and being controlled by the input/output processor" (emphasis added). The hierarchical input/output system disclosed in Eide does not allow for control of an IOA by the system processor. By contrast, the present invention advantageously enables the system processor itself to dynamically assume control of an IOA, potentially making available additional I/O processing capacity in cases where, for example, an IOP has failed, or the IOP's in operation are otherwise busy. Accordingly, it is respectfully submitted that claim 1 patentably distinguishes over the applied Eide reference.

Regarding independent claim 4, the Examiner points to Figure 12 of Eide as disclosing a method for fault recovery comprising: detecting a fault in the input/output processor (Figure 12, element 182); and switching the input/output

adapter to control by the system processor if the input/output adapter is being controlled by the input/output processor when the fault is detected (Figure 12, element 184). However, element 184 recites the step, "select another IOP to handle the IOA handled by failed IOP" (emphasis added). Contrary to the Examiner's arguments, Figure 12 of Eide fails to teach "switching the input/output adapter to control by the system processor if the input/output adapter is being controlled by the input/output processor when the fault is detected" (emphasis added), as claim 4 requires.

Regarding independent claim 12, the Examiner points to Figure 13 of Eide as disclosing a method for optimizing processor utilization comprising: determining computer system utilization (Fig. 13, element 190, and column 11, lines 6-9); and switching control of the input/output adapter from a first one of the system processor and the input/output processor to a second one of the system processor and the input/output processor (Fig. 13, element 196), if it is determined that the first one of the processors is being over utilized (Fig. 13, element 194) and that the second one of the processors has sufficient capacity that switching control of the input/output adapter will not adversely affect system throughput (Fig. 13, element 196, 198). However, elements 192, 194 and 196 of Figure 13 respectively recite the steps "periodically receive performance data from each IOP," "IOP workloads unbalanced?" and "select IOA to transfer between IOP's" (emphasis added). Contrary to the Examiner's arguments, Figure 13 of Eide fails to teach "switching control of the input/output adapter from a first one of the system processor and the input/output processor to a second

one of the system processor and the input/output processor" (emphasis added), as claim 12 requires. As in the case of claim 1, the Examiner's arguments regarding claims 4 and 12 fail to recognize that the system processor and the input/output processor are separate and distinct elements of the invention, and that the hierarchical input/output system disclosed in Eide does not allow for control of an IOA by the system processor. Accordingly, it is respectfully submitted that independent claims 4 and 12 also patentably distinguish over the applied Eide reference.

Without prejudice to the traversal by the Applicant of the Examiner's rejection, claims 1, 4 and 12 are amended herein solely for the purpose of more clearly reciting the invention.

It is submitted that claims 2-3, 5-11 and 13-17 are allowable for at least the reason that they depend from the independent claims 1, 4 and 12. Further, these dependent claims recite other features that independently distinguish over the applied prior art. For example, claims 2, 5, 9 and 16 recite the limitation, "wherein the input/output adapter is a PCI (Peripheral Component Interconnect) adapter," while claims 3, 6, 10 and 17 recite the limitation, "wherein the input/output processor is a PCI-compatible processor." In regard to these claims, the Examiner points generally to Figure 2, elements 44 and 48, which are identified generically in the figure as an input/output processor (IOP) and an input output adapter (IOA), respectively. What Figure 2 does not disclose is that these devices are specifically a PCI-compatible processor and a

PCI adapter. As would be understood by those of ordinary skill in the art, PCI is a standard developed by Intel Corporation for local data busses that connect directly to the system processor used in a personal computer (PC). Eide refers to a number of network protocols used by peripheral devices to communicate (see, generally, column 5, lines 10-25), but does not disclose the PCI bus protocol as being used between the IOP's and IOA's.

Regarding claim 8, the Examiner points to Eide (column 10, lines 38-40) as disclosing the step, "switching the input/output adapter to control by the input/output processor when the correction of the default is detected, if it was previously switched to control by the system processor as a result of the fault in the input/output processor." However, while the referenced text does discuss reassigning IOA's in response to a detected failure in an IOP, it fails to disclose the additional step, addressed in claim 8, of switching control back to the IOP when the fault is corrected. The same argument applies to the Examiner's rejection of claim 11.

Regarding claim 13, the Examiner points to Eide (Figure 13, and column 11, lines 9-15) as disclosing the limitation, "wherein switching control of the input/output adapter from the first one of the processors to the second one of the processors is further based on a determination that the over utilization of the first of the processors is likely to continue for at least a specified period of time." The referenced text discusses using measured IOP performance data to determine whether the IOP work loads are significantly unbalanced. Eide states that

various algorithms may be used in block 194 of Figure 13 to determine such a condition. The example give is detecting an unbalanced condition when the utilization of one IOP is greater than a given threshold while the utilization of another IOP is below another threshold. However, Eide fails to teach or suggest reassigning an IOA "based on a determination that the over utilization of the first of the processors is likely to continue for at least a specified period of time," as claim 13 requires. The same argument applies to the Examiner's rejection of claim 11. Nor does the referenced text in Eide teach the further limitation "wherein the steps of determining computer system utilization and switching control of the input/output adapter based on such determination are repeated at intervals substantially equal to the specified period of time," as recited in claim 14. Eide simply states that IOP performance is monitored periodically (see column 11, lines 1-6), without indicating in any way how that period might be specified.

New dependent claim 18 is directed to subject matter disclosed in the application (see application Figure 1, and page 6, lines 4-5), but not specifically addressed in the original claims.

It should be noted that the Eide patent and the present invention have both been assigned to IBM Corporation and therefore, Eide is not applicable as prior art to preclude patentability under 35 U.S.C. §103.

It is respectfully submitted that the application, as now amended, is in condition for allowance. Notice of allowance and the passing of the application

to issue are respectfully solicited.

If the Examiner believes that a conference would be of value in expediting the prosecution of this application, the Examiner is hereby invited to telephone the undersigned counsel to arrange for such a conference.

Respectfully submitted,

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Date

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